High-Speed and Low-Power GaAs Phase Frequency Comparator

KAZUO OSAFUNE, KUNIKI OHWADA, AND NAOKI KATO

Abstract—**A high-speed and low-power consumption phase frequency comparator (PFC) for a phase lock stable oscillator was designed and fabricated with a GaAs MESFET BFL circuit for the first time. The threshold voltage, gate width, and gate length of GaAs MESFET's in the PFC were determined by circuit simulations for a high-speed and low-power operation. The fabrication process used buried p-layer SAINT-FET's with 0.5-μm gate length. The fabricated PFC performed stable phase and frequency comparison up to 600 MHz at only 60 mW. Using dislocation-free wafers, the fabrication yield in the laboratory was more than 90 percent.**

I. INTRODUCTION

SINCE the recent progress of GaAs logic IC high-speed operation and enlargement is remarkable, and the application to various fields has proceeded [1]. Regarding a local oscillator circuit of satellite [2] or microwave communication systems, the applications of GaAs IC's have been made owing to these characteristics of high-speed operation, low-power consumption, and radiation hardness. The schematic diagram of a stabilized local oscillator system is shown in Fig. 1. In the local oscillator using the stabilization of a voltage controlled oscillator (VCO), a phase frequency comparator (PFC) that controls a VCO by comparing the divided frequency of VCO to the output frequency of a stable oscillator, such as a crystal oscillator, is necessary. A PFC is a circuit which puts out a control signal detecting the difference of phase and frequency of two input signals. A conventional PFC, for example Motorola MC12040, has been fabricated using Si ECL technology [3]. A typical operating frequency is only 80 MHz and its power consumption is in excess of 300 mW. To simplify the construction of a phase lock loop, to enlarge phase and frequency stability, and to reduce consuming power, a PFC operating at higher frequency with lower power is neccessary. Consequently, a high-speed and low-power PFC using a GaAs IC is urgently required.

In this paper, the first attempt at a GaAs high-speed and low-power PFC is described. As for the basic gate, a GaAs BFL using only a normally-on FET is advantageous from the viewpoints of high-speed operation, large operation margin, strong performance against large fan-out, and easy fabrication using only a normally-on FET [4], [5]. Here we adopted a BFL circuit with a source follower expected for high-speed operation as a basic gate [6], designed a high-speed and low-power consumption PFC, and fabricated

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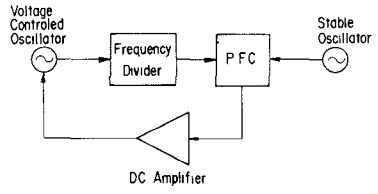


Fig. 1. Schematic diagram of a stabilized local oscillator system.

PFC IC's. Circuit simulations of the PFC operation were nade regarding FET threshold voltage, gate width and gate ength, and the prospect for higher speed operation was shown. The fabrication process used electron beam lithography to shorten the gate length and newly developed buried p-layer SAINT(BP-SAINT) [7], which made high transconductance (g_m) FET's. The fabricated PFC performed a stable phase and frequency comparison operation up to 600 MHz at only 60 mW. Thanks to the use of dislocation-free wafers [8] and fabrication process advancement, the fabrication yield was higher than 90 percent. A corresponding 17-stage ring oscillator circuit showed minimum propagation delay of 44 ps at 16.5 mW/gate, and also a 92 percent yield was attained.

II. CIRCUIT DESIGN

A logic diagram of a PFC is shown in Fig. 2 [3]. The PFC is constructed with nine NOR gates. As the basic gate, as mentioned before, we used a BFL circuit with a source follower as shown in Fig. 3 which enabled large driving capability and high speed. In the circuit, the gate widths of FET's and diodes are equal to W_g. The PFC was designed using FET and diode models including parasitic capacitances [9] which were fitted to FET and diode characteristics fabricated by a process described later in this paper. The circuit simulations were carried out using SPICE II. The maximum operating frequency at which the PFC could put out the same width pulse as the difference between two input signal phases (a phase comparison performance) and could put out the high or low level according to the difference of two input signal frequencies (a frequency comparison performance), was calculated by circuit simulations, and the PFC was designed. The maximum operating frequency is decided with the critical path of a PFC logic diagram of 18 gates.

First, the simulated result of the relationship between the FET threshold voltage V_t, the maximum operating frequency, and the power consumption is shown in Fig. 4.

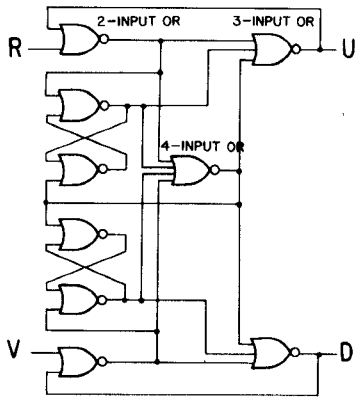


Fig. 2. Logic diagram of a phase frequency comparator.

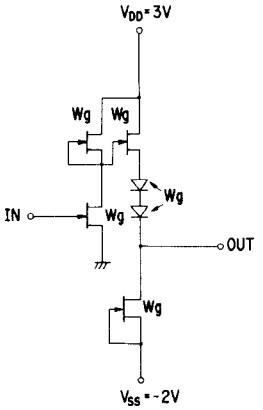


Fig. 3. Schematic diagram of a BFL gate circuit.

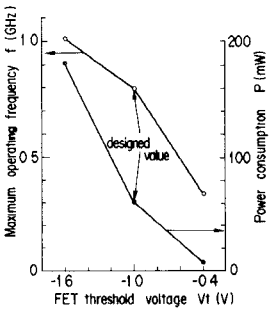


Fig. 4. Simulated relationship between FET threshold voltage, maximum operating frequency, and power consumption ($L_g = 0.5\ \mu$m, $W_g = 10\mu$m).

FET gate width and gate length are 10 and 0.5 μm, respectively. As for the threshold voltage of -0.4, -1.0, and -1.6 V, the numbers of level shift diodes in Fig. 3 are 1, 2, and 3, respectively. One can understand from the figure that, as the threshold voltage becomes low, the maximum operating frequency becomes high; below -1 V, the increasing rate of the maximum operating frequency has been suppressed. The power consumption increases steadily. From this result, the FET threshold voltage of -1 V was adopted in order to obtain low-power consumption and high-speed operation.

The simulated result of the relationship between the FET gate width, and the maximum operating frequency and the power consumption is shown in Fig. 5. The gate length is

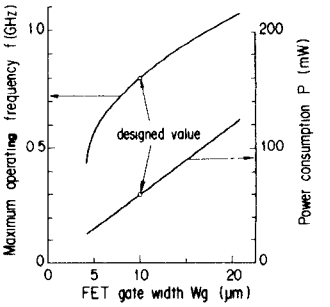


Fig. 5. Simulated relationship between FET gate width, maximum operating frequency, and power consumption ($V_t = -1.0$ V, $L_g = 0.5\ \mu$m).

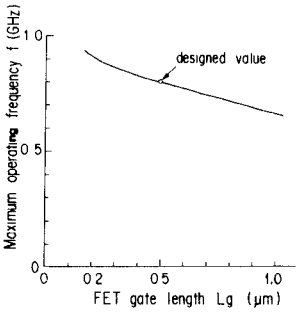


Fig. 6. Simulated relationship between FET gate length and maximum operating frequency ($V_t = -1.0$ V, $W_g = 10\ \mu$m).

0.5 μm. From Fig. 5, one sees that, as the gate width becomes wide, the maximum operating frequency increases, but above 10 μm, the increasing rate of the maximum operating frequency has been suppressed. On the other hand, the power consumption increases linearly. Similarly, to obtain low-power consumption and high-speed operation, we adopted the FET gate width of 10 μm.

The relationship between the FET gate length and the maximum operating frequency is shown in Fig. 6. In this case, FET I–V characteristics are assumed not to vary for the FET gate length, so the power consumption is constant. As the gate length becomes shorter, the maximum operating frequency increases, but the FET of a gate length below 0.5 μm cannot be fabricated stably by the present process. Therefore, a gate length of 0.5 μm was used.

Consequently, in the following, we will report the result of fabrication and measurement of the designed PFC IC's with the FET threshold voltage of -1 V, the gate width of 10 μm, and the gate length of 0.5 μm.

III. IC Fabrication

Gate length shortening is the most effective method to obtain high-performance FET's. However, FET's with submicron gate lengths present undesirable short channel effects, such as the FET threshold voltage V_t reduction, large subthreshold current, and V_t scatter increases. The buried p-layer SAINT process [7] was applied to decrease the short channel effect. As a result, 0.5 μm gate length FET's were successfully fabricated using electron beam lithography. In this process, a p-layer is formed under the active layer to suppress substrate current by Be^+ implantation. Dislocations in LEC grown GaAs crystal induce V_t scatter.

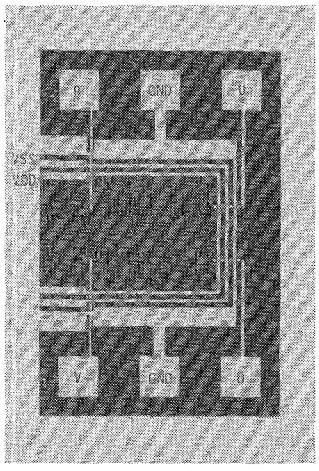


Fig. 7. Micro-photograph of the fabricated PFC (a PFC portion of prescaler with PFC IC chip).

Thus, 2-in-diam dislocation-free wafers were used, which were obtained from the fully encapsulated Czochralski method combined with indium doping [10].

The fabricated FET average threshold voltage $\bar{V}_t$ was -1.17 V from four 2-in-diam wafers, and this standard deviation was suppressed to 75 mV in spite of the short gate length of 0.5 μm. The FET average transconductance $\bar{g}_m$ was 175 mS/mm ($V_{GS} = 0$ V, $V_{DS} = 2.0$ V).

A micro-photograph of the fabricated PFC is shown in Fig. 7. The chip size was 0.5 $\times$ 0.6 mm square. The circuit geometry was optimized to obtain high-speed operation and made compact by a symmetric circuit arrangement and short interconnection.

IV. Performance

A. Transfer Characteristics and Ring Oscillator

As for the transfer characteristics of a BFL basic gate, the transfer gain was 3.5, and the high level and low level were 0.8 and -0.8 V, respectively, at a typical bias condition of $V_{DD} = 3$ V and $V_{SS} = -2$ V. The performance of the 17-stage ring oscillators using BFL circuit of $W_g = 20$ μm was measured. The ring oscillator demonstrated a minimum propagation delay t_{pd} of 44 ps at 16.5 mW/gate. The waveform of the ring oscillator is shown in Fig. 8. This minimum propagation delay corresponds to the simulated value by the above-mentioned model. The 92 percent yield of these ring oscillators was obtained from three wafers. The gate number of the ring oscillator is twice as many as that of the PFC. The histograms of propagation delays and power consumption of the ring oscillators are shown in Fig. 9. As shown in Fig. 9, the average propagation delay was 48.5 ps, and the standard deviation was less than 5.3 ps. The average power consumption was 16.2 mW/gate, and the standard deviation was 4.2 mW/gate, and small. The uniformity was very good. It is supposed that the quality of the yield and the uniformity depended on the large operation margin of the BFL circuit, the use of dislocation-free wafers, and the fabrication process advancement. The relationship between propagation delays

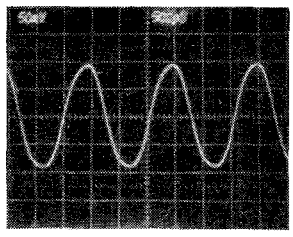
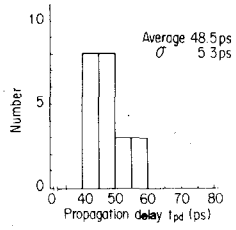
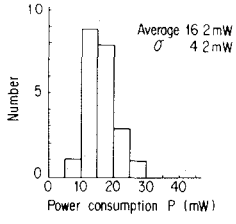


Fig. 8. Waveform of a 17-stage ring oscillator.



(a)



(b)

Fig. 9. Histograms of propagation delays and power consumptions of ring oscillators. (a) Histogram of propagation delays. (b) Histogram of power consumptions.

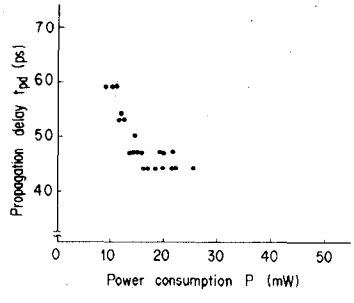


Fig. 10. Relationship between propagation delays and power consumptions.

and power consumption is shown in Fig. 10. It was observed that the larger the power consumptions, the smaller the propagation delay became. The reason for this trend is clear because the current of an FET becomes higher as the FET g_m becomes larger, and the power consumption is greater when propagation delay is smaller.

B. PFC

The maximum operating frequency and power consumption of fabricated BFL PFC's were measured. In this measurement, PFC's were mounted on a 50-Ω coplanar test fixture, and at the inputs R and V of the PFC, 50-Ω chip resistors were attached. The supply voltages were $V_{DD} = 3$

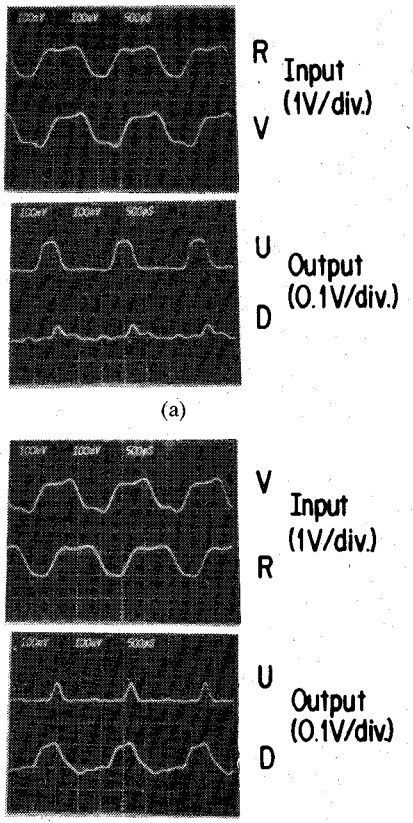


Fig. 11. Pulse performance of a PFC ($f = 600$ MHz). (a) Relationship between inputs and outputs when R led V by 300 ps. (b) Relationship between inputs and outputs when V led R by 300 ps.

V and $V_{SS} = 2$ V. The pulse performance of putting out the same width pulse as the difference between two input signal phases, was measured. The maximum operating frequency was 600 MHz at only 60 mW. The input sensitivity was 0.6 V. These results are at a far higher speed and lower power consumption than the 80-MHz frequency and 300-mW power of the conventional one. The result almost corresponds to the above-mentioned result by the simulation and that of the ring oscillator. The pulse performance is shown in Fig. 11. Fig. 11 (a) shows the relationship between inputs and outputs U and D in the case where R led V, and Fig. 11 (b) shows the same in the case where V led R. The rise and fall times of output are 100 and 200 ps, respectively.

The dc performance was measured by detecting with a dc voltage meter between two terminals of buffer series 500-Ω chip resistors connected at the PFC outputs. The phase comparison performance of the relationship between the difference of the input signal phases and the buffer series 500-Ω chip resistors terminals dc voltage V_{DC} is shown in Fig. 12. From this figure, it is recognized that the output dc voltage varied regularly by a cycle of 2 π owing to the difference between two input signal phases. The dc voltage varied linearly according to the difference between two input signal phases within 2 π. The frequency comparison performance by detecting the dc output voltage in the condition that one input signal frequency was fixed at

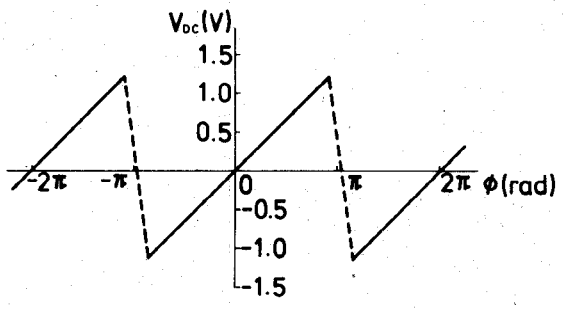


Fig. 12. Phase comparison performance ($f = 600$ MHz).

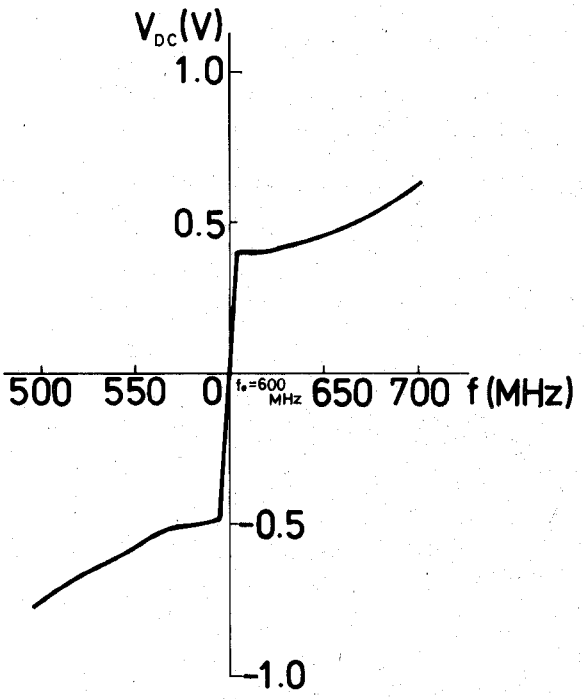


Fig. 13. Frequency comparison performance.

600 MHz and the other input signal frequency was swept is shown in Fig. 13. The output dc voltage changed abruptly from the low level to the high level around 600 MHz.

As described in Section IV-B, it is realized that the PFC performed a stable phase and frequency comparison operation up to 600 MHz at the low-power consumption of 60 mW with more than 90 percent yield. It is supposed that the scatter of the PFC performance was well suppressed considering the scatter of the ring oscillator performance in Fig. 9.

V. Conclusion

The PFC used to stabilize the local oscillator circuit in satellite and microwave communication systems was designed and fabricated for the first time using a GaAs MESFET BFL circuit which enables high-speed operation and large operating margin. The design parameters of FET threshold voltage, gate width, and gate length were optimized for the PFC to enable high-speed operation and low-power consumption. The PFC performed a stable phase frequency comparison operation up to 600 MHz at only 60 mW, which was nearly the expected value by simulations.

The fabrication yield was more than 90 percent owing to the use of dislocation-free wafers and process advancement. By circuit simulations, it was recognized that the PFC with FET gate length of 0.2 μm could operate up to 900 MHz at the same low-power consumption as that with a gate length of 0.5 μm. The corresponding ring oscillator result showed a minimum propagation delay of 44 ps at 16.5 mW/gate, and good uniformity of IC performance was obtained.

As described above, it became clear that the PFC IC using GaAs BFL circuit is currently receiving sufficiently practical application.

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